**ADE7880 Data Sheet Detailed Change List**

New parameter is listed as follows:

1. NEW DEFINITION: "Ttyp", the typical temperature, will be defined as 25°C. Previously Ttyp was not specified.

Parameters changing are listed as follows:

1. ANALOG INPUTS: Gain Error will change:

From: -2% typical

To: +4% typical

1. ON-CHIP REFERENCE: PSM0 and PSM1 Modes Temperature Coefficient will change:

From: 10 ppm/°C typical and 50 ppm/°C maximum

To: -50 ppm/°C minimum, +20 ppm/°C typical and +50 ppm/°C maximum.

1. TIMING CHARACTERISTICS: I2C Data Hold Time, tHD;DAT, in standard and fast mode will change:

From: 0 us minimum

To: 0.1us minimum

Parameters no longer specified are listed as follows:

1. ACTIVE ENERGY MEASUREMENT and REACTIVE ENEGY MEASUREMENT: Phase error between channels will no longer be specified. Previously these parameters were + 0.05 degrees maximum.
2. ON-CHIP REFERENCE: PSM0 and PSM1 Modes Reference Error will no longer be specified. Previously these were +2mV typical.
3. ON-CHIP REFERENCE: PSM0 and PSM1 Modes Output Impedance will no longer be specified. Previously these were 1kΩ minimum.
4. CLKIN: Crystal ESR, CKLIN Load Capacitor and CLKOUT Load Capacitor will no longer be specified. Previously these parameters were 30 Ω minimum / 200 Ω maximum and 20 pF minimum / 40 pF maximum respectively.
5. LOGIC OUTPUTS: ISOURCE and ISINK will no longer be specified for logic output pins. These parameters will, instead, be stated in the comments section.

Clarifications/Comments have been added as follows:

1. RMS MEASUREMENTS: Measurements will be performed in PSM0 mode. Previously this was not specified.
2. MEAN ABSOLUTE VALUE (MAV): Measurements will be performed in PSM1 mode. Previously this was not specified
3. HARMONIC MEASUREMENTS: Added the following Fundamental Line Frequency comments: "Voltage signal must have amplitudes greater than 100 mV peak at ADC stage. Set the SELFREQ bit of COMPMODE register based on the frequency. See the Managing Change in Fundamental Line Frequency section for details"
4. ANALOG INPUTS: Added the following Maximum Signal Level comments: "PGA = 1, differential or single-ended inputs
between the following pins: IAP and IAN, IBP and IBN, ICP and ICN, INP and INN; single-ended inputs between the following pins: VAP and VN, VBP and VN, VCP and VN"
5. WAVEFORM SAMPLING: Added the following Current and Voltage Channels SNR and SINAD comments "PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology section"
6. LOGIC INPUTS and LOGIC OUTPUTS: The supply voltage stated in the comments section has been changed to VDD = 3.3V from VDD=3.3V+10%.
7. LOGIC OUTPUTS-CF1, CF2, and CF3/HSCLK: The sink current used for testing the maximum VoL logic level has been changed from 2mA to 8mA.
8. ON-CHIP REFERENCE: The following comment has been added “Drift across the entire temperature range of −40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more details”.
9. CLKIN: The following comment has been added “See the Crystal Circuit section for more details”.